Progress Report

Grant #731009
Ultra-Efficient Generators & Diesel Electric Propulsion
Genesis Machining & Fabrication
Reporting Dates: 9/2012-12/2012

Deliverables Submitted:

No deliverables due at this time.

Budget:

Item	Cost
GPIC	1508.84
IGBT's	844.56
Total	**2353.4**

We had two expenditures this period for which we are billing. This first is for the General Purpose Inverter Controller (GPIC) board produced by National Instruments. Although NI gave us a free board, we were obligated to purchase a board to receive our Green Grant. This is the OEM board which will be shipped with all of our inverter products. The second expense is for a new set of FUJI IGBT's (insulated gate bipolar-transistor), the main electronic switch component of our inverter.

Schedule Status:

We are on schedule to complete the next milestone by the end of March 2013: Completing the TRL-6 UMIC and EV testbed.

Percent Complete:

We are about 25% complete with the first milestone listed in the grant schedule.

Work Progress:

A lot has happened since our presentation to AEA in August, 2012. The main development has been our $25,000 Green Grant award from National Instruments. We are sure that this serendipitous project component will drastically enhance our products and greatly simplify our development path. This grant comprises a full LabView Development Suite along with Circuit Simluation

and PCB design software. The core technology we are utilizing from NI is the Single-Board Reconfigurable I/O General Purpose Inverter Controller, see Figure 1 below.

Figure 1 - National Instruments GPIC

This OEM board is specifically designed to control high power inverter applications. Its onboard Field Programmable Gate Array (FPGA) provides an easily programmable custom signal processing solution providing up to 40 X the performance of traditional DSP solutions. During this reporting period the grant lead engineer and computer engineer have both participated in online classes provided by NI to learn LabView FPGA programming. Using this knowledge, we have successfully used the GPIC to control our TRL-6 UMIC core.

Goal Met:

Using the NI GPIC we have successfully implemented a prototype control algorithm and data acquisition system using our TRL-6 UMIC core.

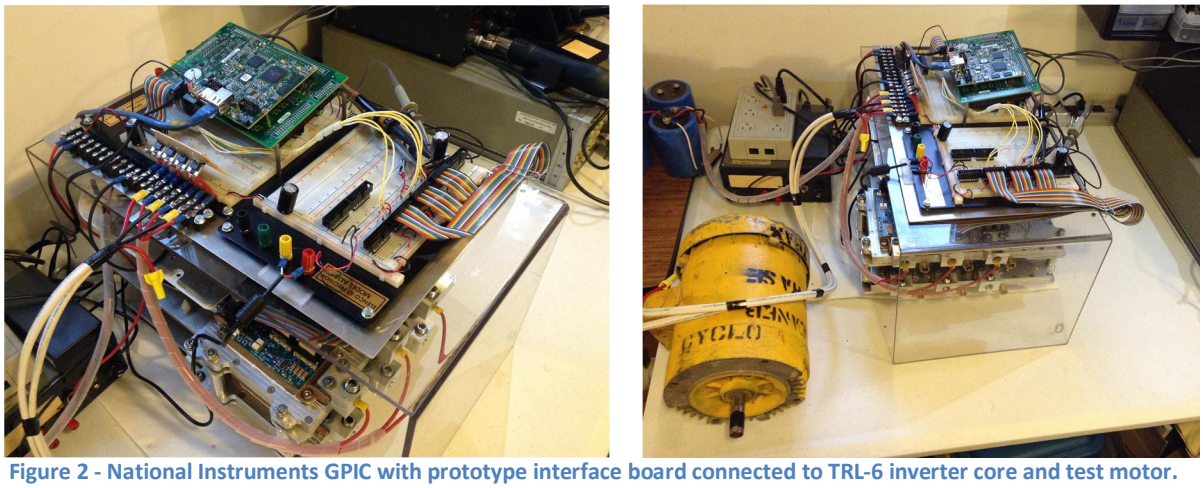

Figure 2 - National Instruments GPIC with prototype interface board connected to TRL-6 inverter core and test motor.

Along with sucessfully controlling a 3-phase motor with the GPIC and TRL-6 core, we have shown 5 nS (200 MHz) timing resolution on data acq. and control signals.

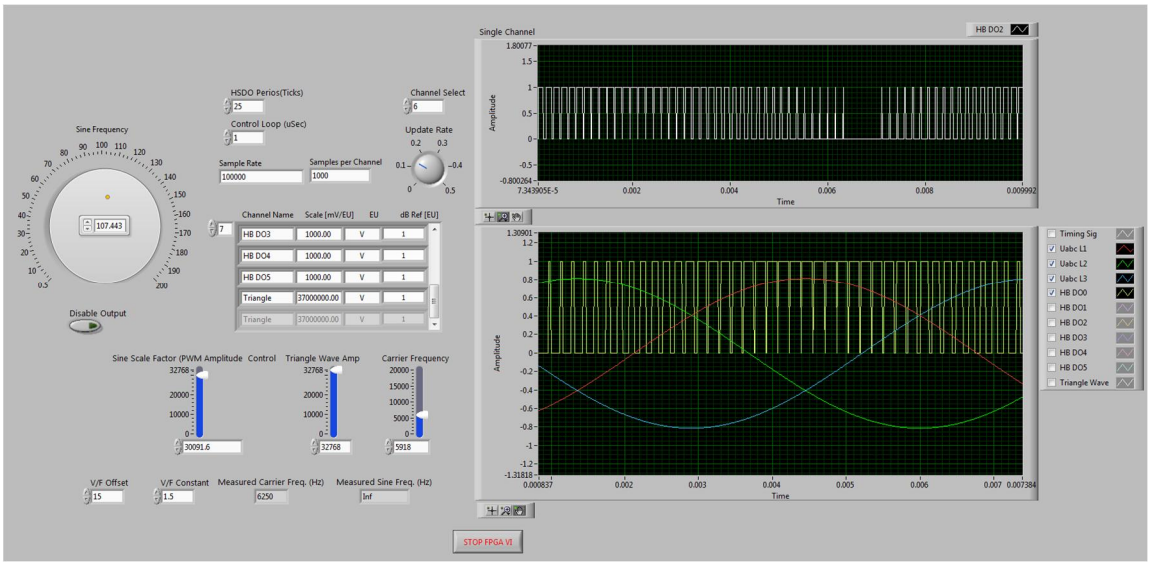

Figure 3 – Graphical front-end for our 3-phase inverter and data-acquisition

To summarize our work progress for this quarter we have:

1) Learned LabView FPGA and successfully transitioned to the GPIC platform.
2) Controlled a 3-phase motor with our TRL-6 core.
3) Confirmed 5 ns timing resolution for data and control signals
4) Identified major data acquisition and isolation IC's
5) Identified battery chemistry for EV test-bed
6) Identified desired 3-phase control algorithm

There were no unexpected problems this quarter. The only slow area was learning LabView FPGA, but the initial, difficult learning curve has already yielded major paybacks!

In addition to the Green Grant from NI, we also received a free GPIC board from NI (a $1500 value), and Agile Switch will be providing us with 6 free IGBT driver cores (a $900 value) when they become available later in January. Altogether we have received $27,400 in free hardware and software during this period from our Grant Partners!

Future Work:

The primary goals for the next reporting period are: 1) completing our prototype GPIC to Inverter interface board, 2) implementing a Space Vector Modulation (SVM) algorithm on the GPIC FPGA, and 3) integrating the inverter, battery, and components into the EV test-bed.

We are anticipating that developing the SVM algorithm will be the most challenging aspect of our goals for the upcoming quarter. As far as our research has shown, SVM is the most powerful three-phase control algorithm available but is also the most computationally intensive. We plan on leveraging the FPGA's signal processing power to accomplish this goal, but it will undoubtedly require some tricky programming.